System Memory and I/O Interaction

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Memory Overview

- The **memory** system is the area in the PLC's CPU where all of the sequences of instructions, or *programs*, are stored and executed by the processor to provide the desired control of field devices.

- The memory sections that contain the control programs can be changed, or reprogrammed, to adapt to manufacturing line procedure changes or new system start-up requirements.

Memory Overview

- The total memory system in a PLC is actually composed of two different memories
  - The executive memory
  - The application memory

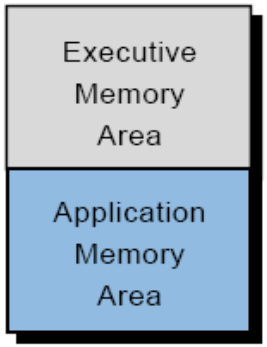

Figure 5-1. Simplified block diagram of the total PLC memory system.

Memory Types

- **Read-only memory (ROM)**
- **Random-access memory (RAM)**
- **Programmable read-only memory (PROM)**
- **Erasable programmable read-only memory (EPROM)**
- **Electrically alterable read-only memory (EAROM)**
- **Electrically erasable programmable read-only memory (EEPROM)**

Memory Structure and Capacity

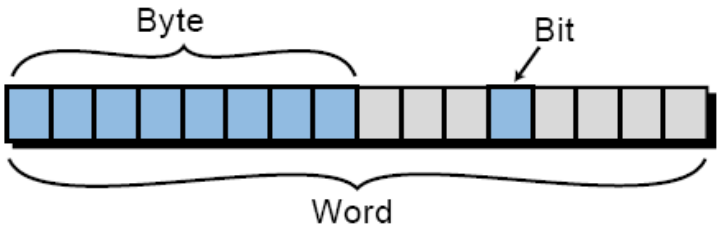

Figure 5-4. Units of PLC memory: bits, bytes, and words.

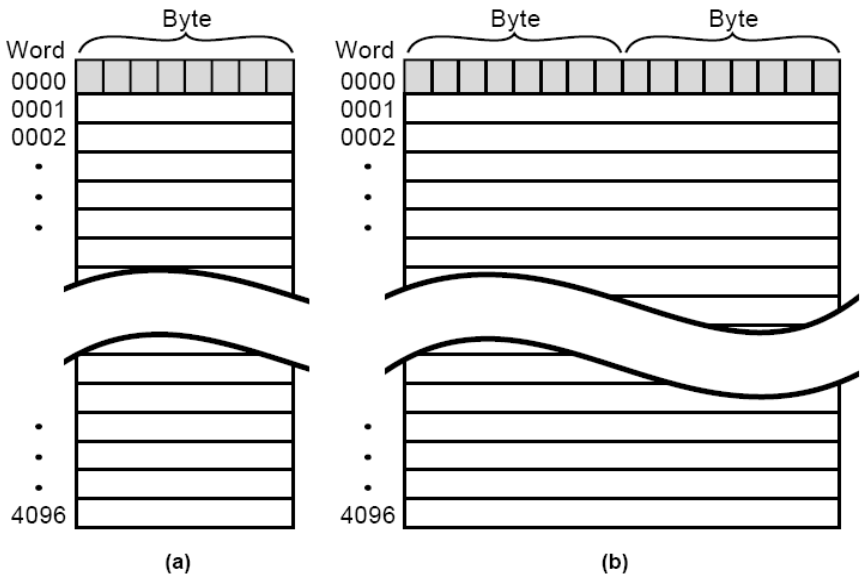

Figure 5-5. Block illustration of **(a)** a 4K by 8 bits storage location and **(b)** a 4K by 16 bits storage location.

Memory Organization and I/O Interaction

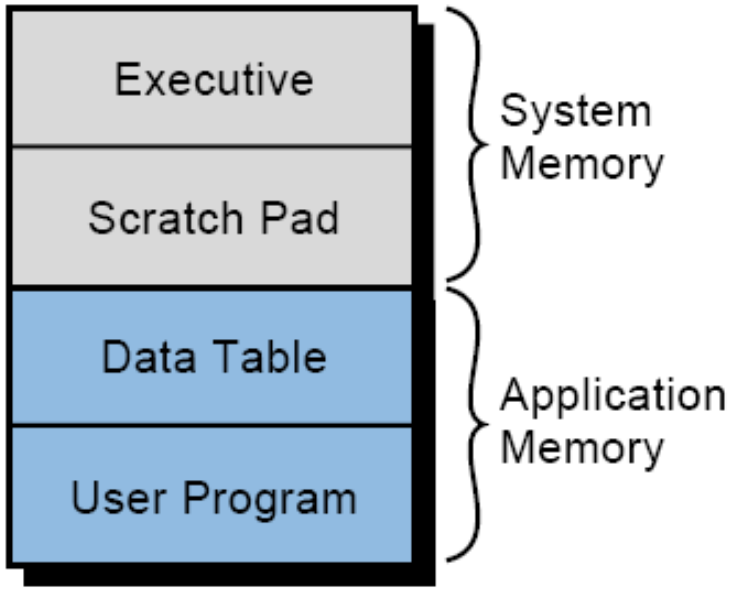

Figure 5-6. A simplified memory map.

- **Executive Area.** Permanently stored collection of programs that are part of the system. These programs direct system activities, such as execution of the control program and communication with peripheral devices.
- **Scratch Pad Area.** Temporary storage area used by the CPU to store small amount of data for interim calculations and Control that are needed for quick access.

Memory Organization and I/O Interaction

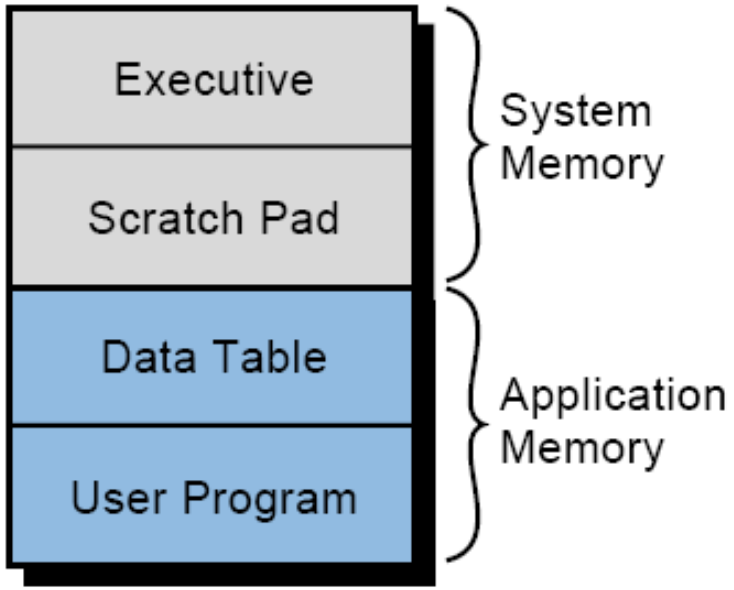

Figure 5-6. A simplified memory map.

- **Data Table Area. S**tores all data associated with the control program, such as timer/counter preset values. The data table also retains the status information of both the system inputs and the system outputs.
- **User Program Area.** This area provides storage for programmed instructions entered by the user. The user program area also stores the control program.

Memory Organization and I/O Interaction

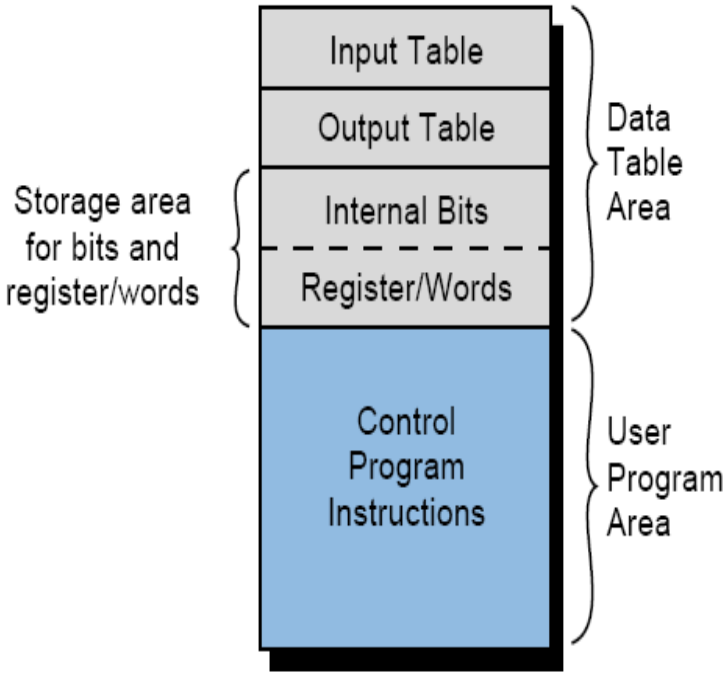

Figure 5-7. Application memory map.

- The **input table** is an array of bits that stores the status of digital inputs connected to the PLC's input interface.
- The **output table** is an array of bits that controls the status of digital output devices that are connected to the PLC's output interface.
- The purpose of the **storage area** section of the data table is to store changeable data, whether it is one bit or a word (16 bits).

Input Table

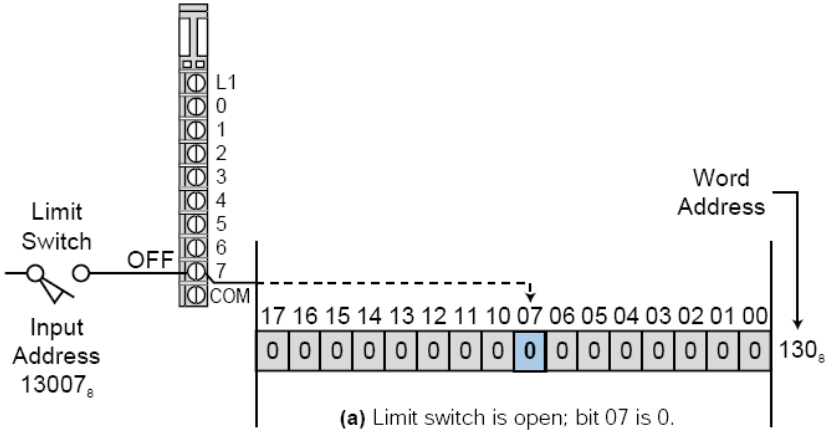

Figure 5-8. Limit switch connected to a bit in the input table.

Output Table

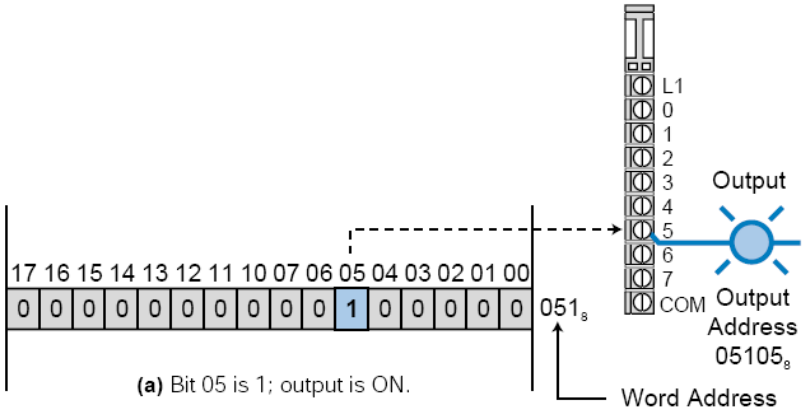

Figure 5-9. Field output connected to a bit in the output table.

Storage Area

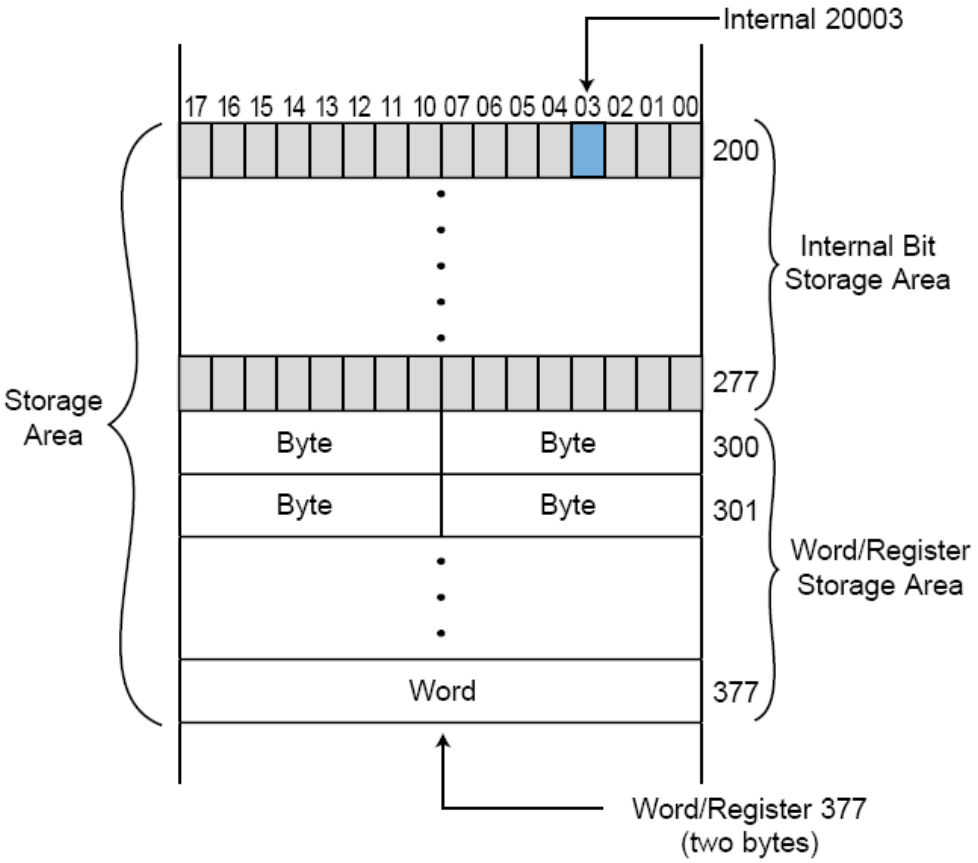

Figure 5-10. Storage area section of the data table.

Storage Area

Constants	Variables
Timer preset values	Timer accumulated values
Counter preset values	Counter accumulated values
Loop control set points	Result values from math operations
Compare set points	Analog input values
Decimal tables (recipes)	Analog output values
ASCII characters	BCD inputs
ASCII messages	BCD outputs
Numerical tables	

Table 5-2. Constants and variables stored in register/word storage area registers.

Example

Referencing Figure 5-11, what happens to internal 2301 (word 23, bit 01) when the limit switch connected to input terminal 10 closes?

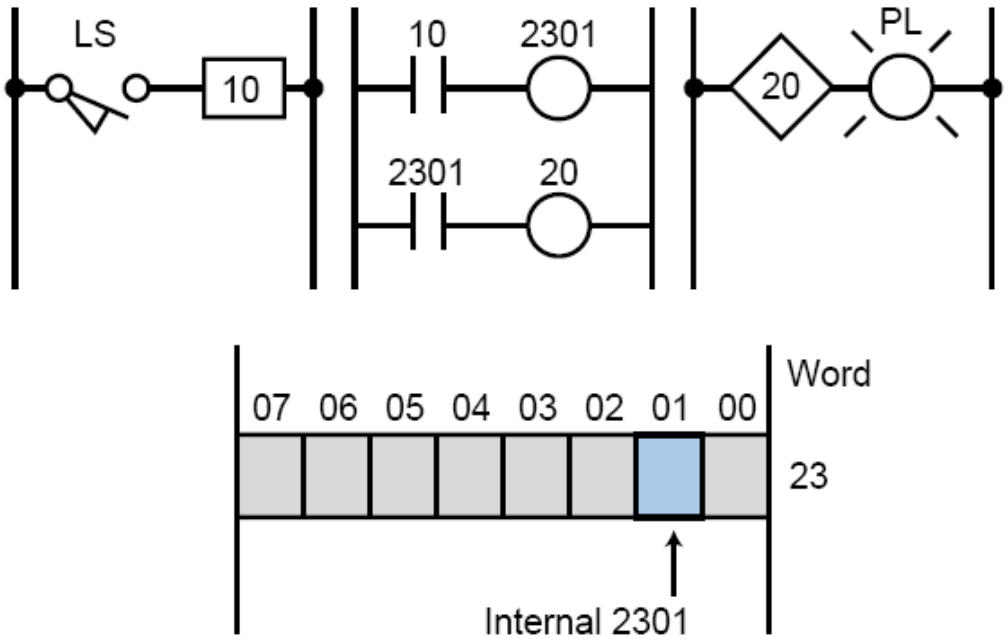

Figure 5-11. Open limit switch connected to an internal output.

Example

When LS closes (see Figure 5-12), contact 10 will close, turning internal output 2301 ON (a 1 in bit 01 of word 23). This will close contact 2301 (⊣2301⊢) and turn real output 20 ON, causing the light PL to turn ON at the end of the scan.

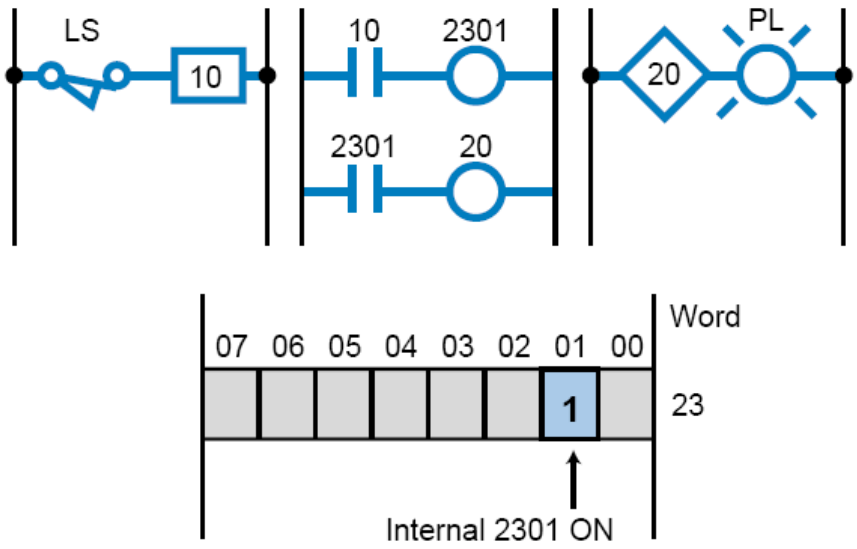

Figure 5-12. Closed limit switch connected to an internal output.

Example: Data Table Organization

- A controller has the following memory, I/O, and numbering system specifications:
  - Total application memory of 4K words with 16 bits
  - Capability of connecting 256 I/O devices (128 inputs and 128 outputs)
  - 128 available internal outputs
  - Capability of up to 256 storage registers, selectable in groups of 8-word locations, with 8 being the minimum number of registers possible (32 groups of 8 registers each)
  - Octal (base 8) numbering system with 2-byte (16-bit) word length

Example: Data Table Organization

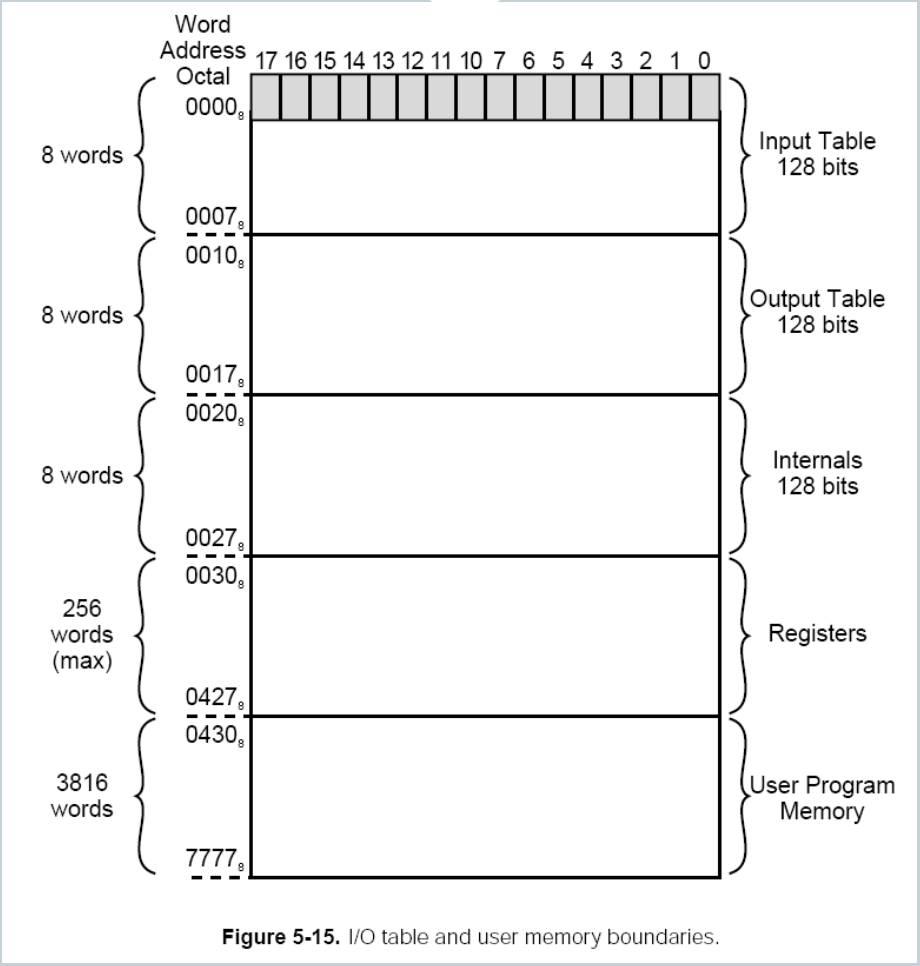

Figure 5-15. I/O table and user memory boundaries.

I/O Addressing

Figure 5-17. A relay circuit with a limit switch driving a pilot light.

I/O Addressing

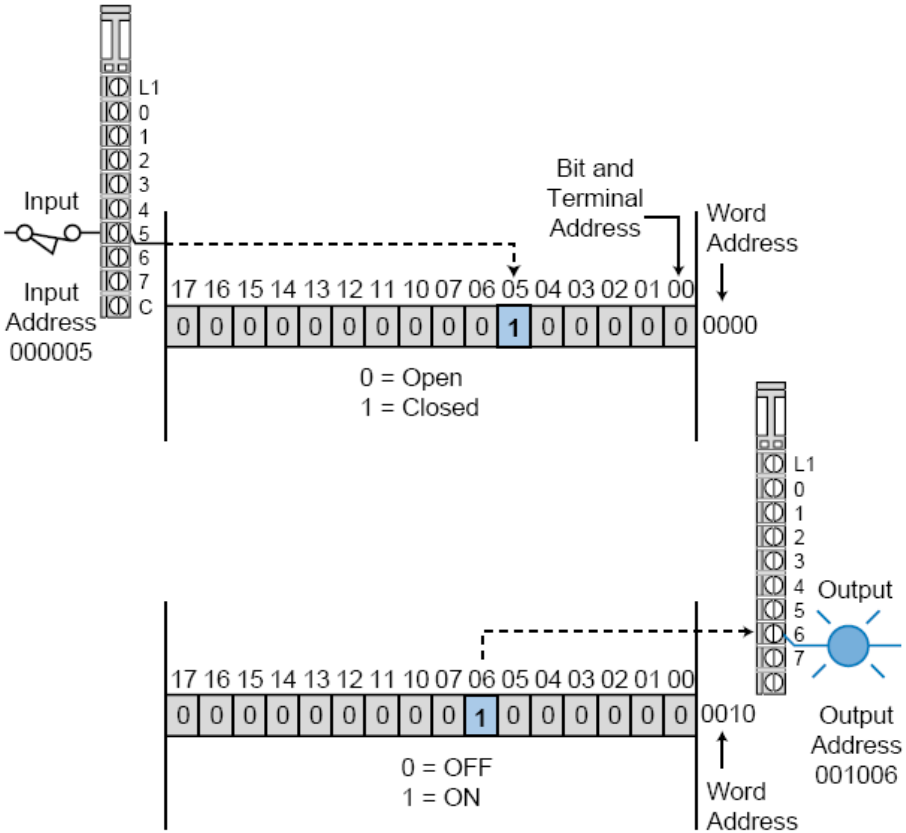

Figure 5-18. Input/output module connected to field devices.

I/O Addressing

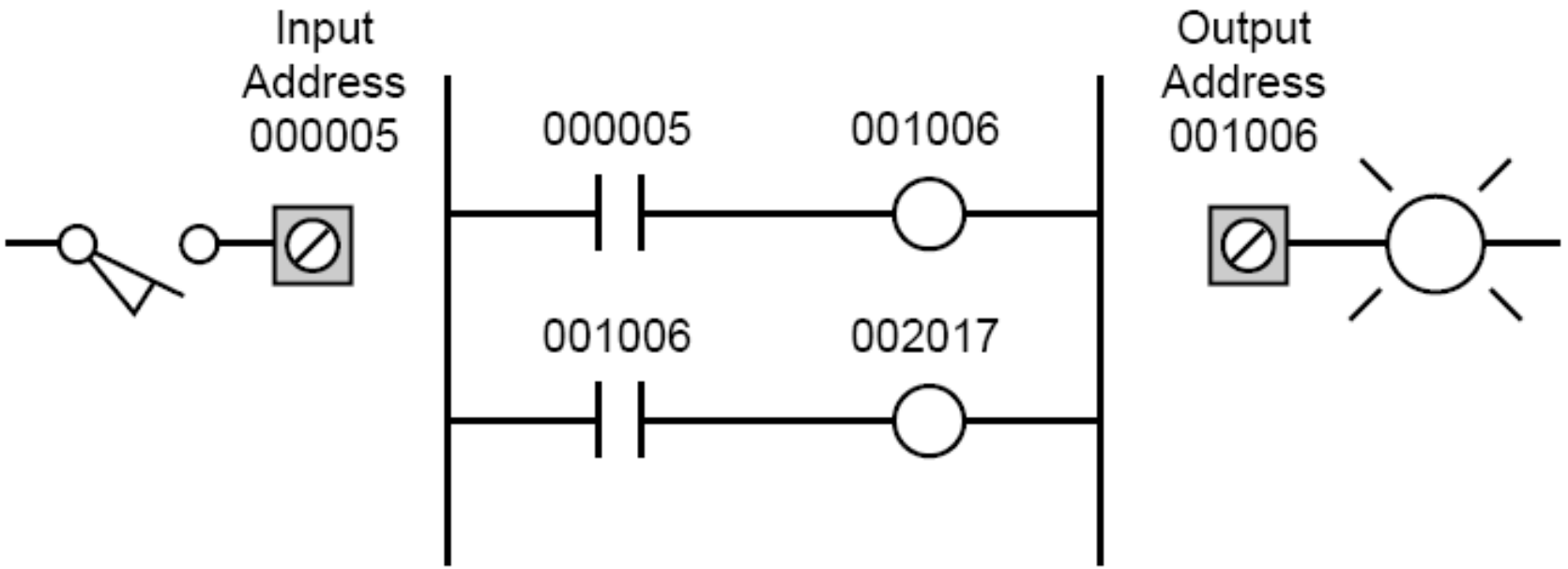

Figure 5-19. PLC ladder implementation of Figure 5-17 using an internal output bit.

I/O Interaction

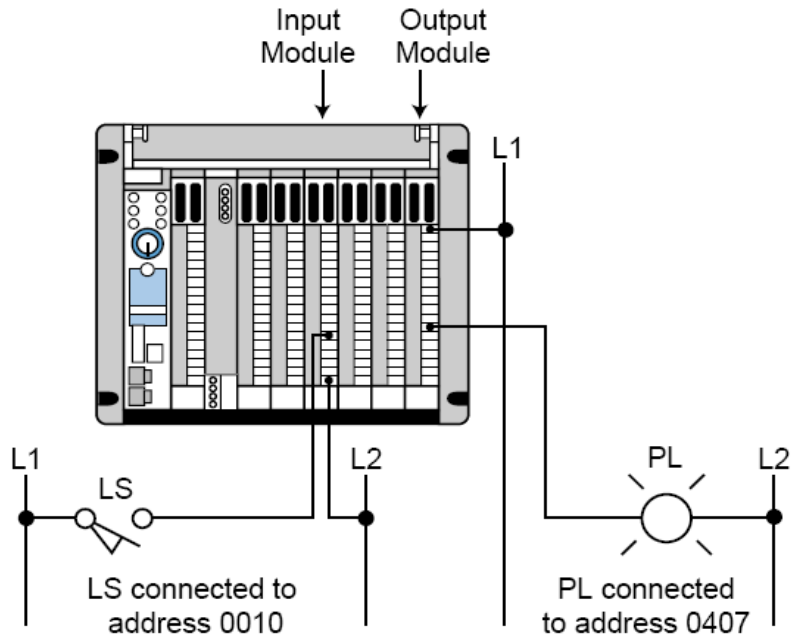

Figure 5-21. A simple circuit connected to a PLC via I/O interfaces.

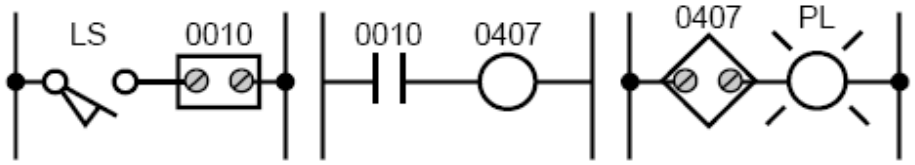

Figure 5-22. Instructions used to represent the control program.

Reference: Programmable Controllers: Theory and Implementation by Bryan and Bryan